

IN THE CLAIMS

What is claimed is:

- 1 1. A semiconductor apparatus, comprising:
  - 2 a plurality of device elements formed on a surface of a semiconductor
  - 3 substrate, each device element having a diffusion region; and
  - 4 a multi-layer wiring configuration electrically connecting at least two
  - 5 of the diffusion regions, the multi-layer wiring configuration containing a
  - 6 plurality of wiring layers, a first wiring layer of the plurality of wiring layers
  - 7 being divided into a first wiring region for providing wiring in a first direction
  - 8 and a second wiring region for providing wiring in a second direction.
- 1 2. The semiconductor apparatus according to claim 1, wherein the first direction is
- 2 orthogonal to the second direction.
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- 1 3. The semiconductor apparatus according to claim 2, wherein:
  - 2 predetermined wiring in the first wiring layer is electrically connected
  - 3 to and disposed in parallel with wiring in a second wiring layer of the plurality
  - 4 of wiring layers; and
  - 5 the second wiring layer has a higher sheet resistance than the first
  - 6 wiring layer.

1    4.    The semiconductor apparatus according to claim 2, wherein the first wiring layer  
2    includes:

3                a first wiring trace in the second wiring region disposed in the second  
4                direction;

5                a second wiring trace in the second wiring region disposed in the second  
6                direction and separated from the first wiring trace in the first direction; and

7                a third wiring trace in the first wiring region disposed in the first direction and  
8                electrically connecting the first wiring trace and the second wiring trace.

1    5.    The semiconductor apparatus according to claim 2, further including:

2                a memory array having bit lines formed with a second wiring layer;

3                the second wiring layer has a higher sheet resistance than the first wiring  
4                layer.

1    6.    The semiconductor apparatus according to claim 5, wherein the memory array has  
2    dynamic random access memory cells having a capacitor over bit line structure.

1    7.    A semiconductor apparatus, comprising:

2                a plurality of functional circuit blocks, each functional circuit block  
3                including a plurality of device elements, a first wiring region and a second  
4                wiring region; and

5                a multi-layer wiring configuration containing a plurality of wiring  
6                layers for electrically connecting predetermined ones of the device elements,

7       the multi-layer wiring configuration including a first wiring layer disposed in  
8       the first wiring region providing first wiring in a first direction and the first  
9       wiring layer disposed in the second wiring region providing second wiring in  
10      a second direction.

1       **8.**      The semiconductor apparatus according to claim 7, wherein the first direction is  
2       orthogonal to the second direction.

1       **9.**      The semiconductor apparatus according to claim 8, comprising:  
2                    predetermined first wiring in the first wiring layer is electrically  
3                    connected to and disposed in parallel with wiring in a second wiring layer of  
4                    the plurality of wiring layers; and  
5                    the second wiring layer has a higher sheet resistance than the first wiring  
6                    layer.

1       **10.**     The semiconductor apparatus according to claim 9, wherein the second wiring layer  
2       has a higher melting point than the first wiring layer.

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1       **11.**     The semiconductor apparatus of claim 8, wherein the plurality of functional circuit  
2       blocks are disposed in a matrix on the surface of a semiconductor substrate.

1       **12.**     The semiconductor apparatus of claim 8, further including:  
2                    a memory array having bit lines formed with a second wiring layer;

the second wiring layer has a higher sheet resistance than the first wiring layer.

13. The semiconductor apparatus of claim 8, wherein the device elements are insulated gate field effect transistors (IGFETs), each IGFET having a source/drain diffusion region and the multi-layer wiring structure electrically connects a source/drain region of at least two IGFETs within a functional circuit block by using the first wiring layer in the first wiring region and the second wiring region.

14. A method for forming a semiconductor apparatus by electrically connecting functional blocks with a multi-layer wiring configuration containing a plurality of wiring layers and each functional block includes a plurality of device elements, comprising the steps of:

forming a diffusion layer associated with device elements on the surface of the substrate;

forming a first interlayer film;

forming a first wiring layer to produce electrodes electrically connected to the diffusion layer;

forming a second insulation film; and

forming a second wiring layer wherein for each functional block a first wiring region provides electrical connections using the second wiring layer in a first direction only and a second wiring region provides electrical connections using the second wiring layer in a second direction only thereby

15 providing electrical connections between at least two device elements with the  
16 second wiring layer through the electrodes produced by the first wiring layer.

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1 15. The method according to claim 14, wherein the first direction is orthogonal to the  
2 second direction.

1 16. The method according to claim 15, wherein the first wiring layer has a higher sheet  
2 resistance than the second wiring layer.

1 17. The method according to claim 15, wherein at least a portion of the wiring formed by  
2 the second wiring layer in the first wiring region is disposed in parallel and electrically  
3 connected to wiring formed by the first wiring layer producing the electrodes.

1 18. The method according to claim 15, wherein the plurality of functional blocks are  
2 disposed in a matrix on the surface of a semiconductor substrate.

1 19. The method according to claim 15, wherein the step of forming the first wiring layer  
2 also forms bit lines in a semiconductor memory array.

1 20. The method according to claim 19, wherein memory cells in the semiconductor  
2 memory array are DRAM cells having a capacitor over bit line structure and the first wiring  
3 layer has a higher melting point than the second wiring layer.

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